IN THE SPECIFICATION

Please amend the paragraph starting on page 15, line 15 as follows:

-- Once the trench 52 is filled with the isolation oxide 58, the oxide 58 may be patterned such that a shallow cavity 60 is formed along the walls of the channel as indicated in Fig. 4. It should be understood that while the term "cavity" is used to describe the opening formed in the oxide 58, the term is simply used for clarity such that it is easily distinguishable from the trench 52. As can be appreciated, the cavity 60 may also be described as a trench formed in the oxide 58 that extends through the length of the trench 52. In the present exemplary embodiment, the isolation oxide 58 may be etched to form an inverted U-shaped cavity, as illustrated in Fig. 4. In accordance with one exemplary embodiment, each of the plurality of cavities 60 has a depth in the range of approximately 300 angstroms to 1500 angstroms. Further, in accordance with another exemplary embodiment, each cavity 60 may have an aspect ratio of less than or equal to approximately 0.5 to 10. In accordance with another exemplary embodiment, each cavity 60 may have an aspect ratio of less than or equal to approximately 1 to 3. As will be illustrated further below, the exposed edge 62 will form a diode junction[[s]] for the FET 32 having a low junction leakage based on its proximity to the isolation oxide 58. As used herein, the "exposed edge 62" refers to the edge being essentially free of any film, especially oxides and hydrocarbons. --

Please amend the paragraph starting on page 15, line 11 as follows:

-- Once the wordline layers (i.e., oxide 54, polysilicon gate 70 and cap 72) are disposed, the wordlines may be patterned and etched by a conventional means. Next, a nitride layer may be

disposed and etched to form the nitride spacers 74. After formation of the nitride spacers 74, a number of dielectric layers, such as TEOS and BSPG layers, illustrated collectively as dielectric layers 76, may be disposed over the wordline stacks, thereby burying the wordlines. The structure may then be planarized by chemical mechanical planarization (CMP). Next contact holes are formed through the BPSG layers such that openings to the drain 36 and source 38 are formed. Finally, a conductive material, such as a polysilicon plug 80 may be disposed into the holes to provide contacts to the source and drain and metal trace layers (not shown) may be formed on the surface of the dielectric layers 76. The formations of the contact holes may include multiple etch and/or punch steps. For instance, one or more punch steps and/or one or more etch steps, such as a dry etch, may be implemented to etch through the dielectric layers 76 to the underlying source 38 and drain 36. Advantageously, the techniques described herein allow the plugs 80 to be disposed further from the polysilicon gate 70 since the width of the source 38 and drain 36 may be increased. In accordance with one exemplary embodiment, each of the conductive posts or plugs 80 are coupled to the respective drain 36 and source 38 at a distance from the gate 70 that is greater than 50% of the width of the respective drain 36 and source 38 terminals. By moving the plugs 80 further from the gate 70, shorting between the plugs 80 and the gate 70 may be reduced. --